SPRING 2014 CDA 3101 Homework 1

Date-assigned: Feb 4th, 2014
Due dates: Feb 12th, 2014

You are not allowed to take or give help in completing this assignment. Submit the typewritten PDF or Microsoft Word version of the submission in Sakai website before the deadline. Scanned handwritten submissions will NOT be accepted. **You are given a 24-hour grace period with 20% penalty.** No late submission will be accepted. Exceptions will be made for legitimate reasons communicated well ahead of time. Necessary calculation procedure or explanation MUST be provided in your answer.

Total Points: 100 pts

1 (P56 1.7) [15] <§1.6> Compilers can have a profound impact on the performance of an application. Assume that for a program, compiler A results in a dynamic instruction count of 1.0E9 and has an execution time of 1.1 s, while compiler B results in a dynamic instruction count of 1.2E9 and an execution time of 1.5 s.

a). Find the average CPI for each program given that the processor has a clock cycle time of 1 ns.

b). Assume the compiled programs run on two different processors. If the execution times on the two processors are the same, how much faster is the clock of the processor running compiler A’s code versus the clock of the processor running compiler B’s code?

c). A new compiler is developed that uses only 6.0E8 instructions and has an average CPI of 1.1. What is the speedup of using this new compiler versus using compiler A or B on the original processor?

2 (P165 2.3) [10] <§§2.2, 2.3> For the following C statement, what is the corresponding MIPS assembly code? Assume that the variables f, g, h, i, and j are assigned to registers $s0, $s1, $s2, $s3, and $s4, respectively. Assume that the base address of the arrays A and B are in registers $s6 and $s7, respectively.


3 (P168 2.19) Assume the following register contents:

   $t0 = 0xFFFFFFFF, \quad $t1 = 0x12345678
1) [10] <§2.6> For the register values shown above, what is the value of \( t2 \) for the following sequence of instructions?
   \[
   \text{sll } t2, t0, 44 \\
   \text{or } t2, t2, t1
   \]

2) [10] <§2.6> For the register values shown above, what is the value of \( t2 \) for the following sequence of instructions?
   \[
   \text{sll } t2, t0, 4 \\
   \text{andi } t2, t2, -1
   \]

3) [10] <§2.6> For the register values shown above, what is the value of \( t2 \) for the following sequence of instructions?
   \[
   \text{srl } t2, t0, 3 \\
   \text{andi } t2, t2, \text{0xFFEF}
   \]

4) (P170 2.26) Consider the following MIPS loop:

\[
\text{LOOP: slt } t2, 0, t1 \text{ beq } t2, 0, \\
\text{DONE subi } t1, t1, 1 \\
\text{addi } s2, s2, 2 \text{ j LOOP} \\
\text{DONE:}
\]

1) [10] <§2.7> Assume that the register \( t1 \) is initialized to the value 10. What is the value in register \( s2 \) assuming the \( s2 \) is initially zero?

2) [10] <§2.7> For the loops written in MIPS assembly above, assume that the register \( t1 \) is initialized to the value \( N \). How many MIPS instructions are executed?

5) [10] <§3.2> Assume 185 and 122 are signed 8-bit decimal integers stored in 2’s complement format. Calculate 185–122. Is there overflow, underflow, or neither?

6) (P239 3.24) [15]<§3.5> Write down the binary representation of the decimal number 63.25 assuming the IEEE 754 double precision format.